Electronic Version
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Claims

[c1] A method for manufacturing a device including an n-type device and a p-type device, comprising:
doping a portion of a semiconductor substrate;
forming a gap in the semiconductor substrate by removing at least a portion of the doped portion of the semiconductor substrate; and
growing a strain layer in at least a portion of the gap in the semiconductor substrate.

[c2] The method of claim 1, wherein the strain layer is grown on at least a portion which is substantially directly under a channel of the n-type device.

[c3] The method of claim 1, wherein the strain layer is grown on at least a portion which is substantially directly under at least one of a source region or drain region of the p-type device.

[c4] The method of claim 3, wherein the strain layer is not grown under a channel of the p-type device.

[c5] The method of claim 1, further comprising/depositing a patterned photo-resist layer on a semiconductor substrate, wherein the step of depositing comprises:

depositing a photo-resist layer which covers a portion of the semiconductor substrate which is to be under a channel of the p-type device.

[c6] The method of claim 5, wherein the photo-resist layer exposes a portion of the semiconductor substrate which is to be under a channel of the n-type device.

[c7] The method of claim 1, wherein the gap is a tunnel formed under the channel of an n-type device.

[c8] The method of claim 1, further comprising removing the deposited patterned photo-resist layer.

[c9] The method of claim 8, further comprising depositing a mask on the semiconductor substrate.

[c10] The method of claim 9, further comprising patterning the deposited mask such that a portion of the semiconductor substrate is covered and a portion of the semiconductor substrate is exposed.

[c11] The method of claim 10, wherein the step of forming a gap comprises etching the exposed portion of the semiconductor substrate to selectively expose a side-wall of at least a portion of the doped region of the semiconductor substrate.

[c12] The method of claim 11, further comprising depositing a

spacer material over the semiconductor substrate.

[c13] The method of claim 12, wherein the depositing of the spacer material includes depositing the spacer material on exposed portions of the gap.

[c14] The method of claim 13, further comprising filling unexposed portions of the gap with oxide material.

[c15] The method of claim 1, wherein the step of doping comprises doping the semiconductor substrate with Ge.

[c16] The method of claim 15, wherein the doping concentration of the Ge is about 1×10^{14} Ge/cm2 to about 1×10^{16} Ge/cm2.

[c17] The method of claim 1, wherein the step of doping comprises doping the semiconductor substrate with at least one of As, B, In, and Sb.

[c18] The method of claim 1, wherein the step of growing a strain layer comprises growing at least one of SiGe, Si_3N_4, SiO_2 and Sio_xN_y in at least a portion of the gap in the semiconductor substrate.

[c19] A method for manufacturing a device including an n-type device and a p-type device, comprising:
growing a strain layer on a semiconductor substrate;
growing a silicon layer above the strain layer;

forming a gap between the semiconductor substrate and the silicon layer by removing at least a portion of the silicon layer and the strain layer from above the semiconductor substrate; and
growing a strain layer in the gap.

[c20] The method of claim 19, wherein the strain layer is grown on at least a portion which is substantially directly under a channel of the n-type device.

[c21] The method of claim 19, wherein the strain layer is grown on at least a portion which is substantially directly under at least one of a source region or drain region of the p-type device

[c22] The method of claim 19, wherein the strain layer is not grown under a channel of the p-type device.

[c23] The method of claim 19, wherein the step of growing a strain layer comprises growing at least one of SiGe, Si_3N_4, SiO_2 and Sio_xN_y on the semiconductor substrate.

[c24] A semiconductor device, comprising:
a semiconductor substrate having at least one gap, extending under a portion of the semiconductor substrate;
a gate stack on the semiconductor substrate; and
a strain layer formed in at least a portion of the gap,
wherein the gap is formed by doping a portion of the

semiconductor substrate and then etching the doped portion of the semiconductor substrate.

[c25] The device of claim 24 wherein the gap is formed prior to forming the gate stack.

[c26] The device of claim 24, wherein the semiconductor device is doped with at least one of Ge, As, B, In and Sb.

[c27] A semiconductor device, comprising:
a semiconductor substrate having at least one gap, extending under a portion of the semiconductor substrate;
a gate stack on the semiconductor substrate; and
a strain layer formed in at least a portion of the one gap, wherein the strain layer is formed only under at least one of a source region and a drain region of the semiconductor device.

[c28] The device of claim 27, wherein the semiconductor device is a p-type device.

[c29] The device of claim 27, wherein the strain layer is made of at least one of silicon germanium or silicon carbide.

[c30] The device of claim 27, wherein the strain layer is between a surface of an upper portion of the semiconductor substrate which faces a surface of a lower portion of the semiconductor substrate.

[c31] The device of claim 27, wherein the strain layer has a thickness of about 1000 Angstroms to about 5000 Angstroms.

[c32] The device of claim 31, wherein a thickness of the channel is about 30 Angstroms to about 200 Angstroms.

[c33] The device of claim 27, wherein the strain layer is formed under both the source region and the drain region of the semiconductor device

[c34] The device of claim 27, wherein the gap has a first width along an upper surface of the semiconductor substrate and a second width below the upper surface of the semiconductor substrate and the second width is larger than the first width.

[c35] The device of claim 27, wherein compressive stresses of about 100 MPa to about 3 GPa exist within the channel of the device.

[c36] The device of claim 27, wherein the strain layer is at least one of SiGe, Si_3N_4, SiO_2 and Sio_xN_y.